Getting Started with SIwave™ CPA: A Package Model

ANSYS, Inc.
Southpointe
2600 Ansys Drive
Canonsburg, PA 15317
ansysinfo@ansys.com
https://www.ansys.com
(T) 724-746-3304
(F) 724-514-9494

Release 2025 R1
January 2025

ANSYS, Inc. and ANSYS Europe, Ltd. are UL registered ISO 9001:2015 companies.

Conventions Used in this Guide

Please take a moment to review how instructions and other useful information are presented in this documentation.

- Procedures are presented as numbered lists. A single bullet indicates that the procedure has only one step.
- Command font is used for:
  - Command line prompts that should be typed exactly as written.
  - Script examples.
- Bold type is used for the following:
  - Names of windows, workspaces, menu commands, and options.
    - Menu commands are often separated by angle brackets. For example, **File** > **Open**.
  - Labeled keys on the computer keyboard. For example, **Enter**.
- Italic type is used for the following:
  - Emphasis.
  - Publication titles.
- The plus sign (+) is used between keyboard keys to indicate that you should press the keys at the same time. For example, “Press **Shift**+**F1**” means to press the **Shift** key and, while holding it down, press the **F1** key also. You should always depress the modifier key or keys first (e.g., **Shift**, **Ctrl**, **Alt**, or **Ctrl**+**Shift**), continue to hold it/them down, and then press the last key in the instruction.

Getting Help: Ansys Technical Support

For information about Ansys Technical Support, go to the Ansys corporate Support website, http://www.ansys.com/Support. You can also contact your Ansys account manager in order to obtain this information.

All Ansys software files are ASCII text and can be sent conveniently by e-mail. When reporting difficulties, it is extremely helpful to include very specific information about what steps were taken or what stages the simulation reached, including software files as applicable. This allows more rapid and effective debugging.

Table of Contents

Table of Contents **Contents-1**

1 - Introduction **1-1**

2 - Setting Up the Design **2-1**

Importing and Saving the Project 2-1

Working with Layers 2-4

Identifying Power and Ground Nets 2-7

3 - SIwave-CPA RLGC Extraction **3-1**

Defining Pin Groups on Power/Ground Nets 3-1

Performing RLGC Extraction 3-5

4 - Viewing CPA RLGC Results **4-1**

Viewing Tabular and SPICE Results 4-1

Viewing Graphical Results 4-3

1 - Introduction

This Getting Started Guide is intended to quickly familiarize you with the capabilities of SIwave's Chip-Package Analysis (CPA) solver.

The CPA solver is a 3D Finite Element Method (FEM)-based solver for fast and accurate extraction of power and signal nets on packages. SIwave-CPA can generate per-bump resolution SPICE models (thousands of bumps) along with user-defined, pin grouped models that include ground bounce behavior. These models consist of a passive RLGC SPICE netlist that includes package-mounted decoupling capacitors and inductors.

CPA models DC resistance and low-frequency inductance and capacitance effects. High-resolution color maps of resistance and inductance aid in package probing, while a comprehensive HTML reporting feature summarizes the layout geometry, setup, and simulation results. CPA models can be seamlessly imported into Ansys RedHawk for Chip + Package cosimulation.

By following the steps in this guide, you will learn how to perform the following tasks using SIwave-CPA:

- Importing a geometric package model
- Setting layer properties
- Identifying power/ground nets
- Specifying parameter settings for the extraction
- Running an SIwave-CPA RLGC extraction
- Reviewing results in tabular, SPICE, and graphical formats

2 - Setting Up the Design

This section explains how to perform the following tasks:

- Importing and saving a project
- Working with layers
- Identifying power/ground nets

Importing and Saving the Project

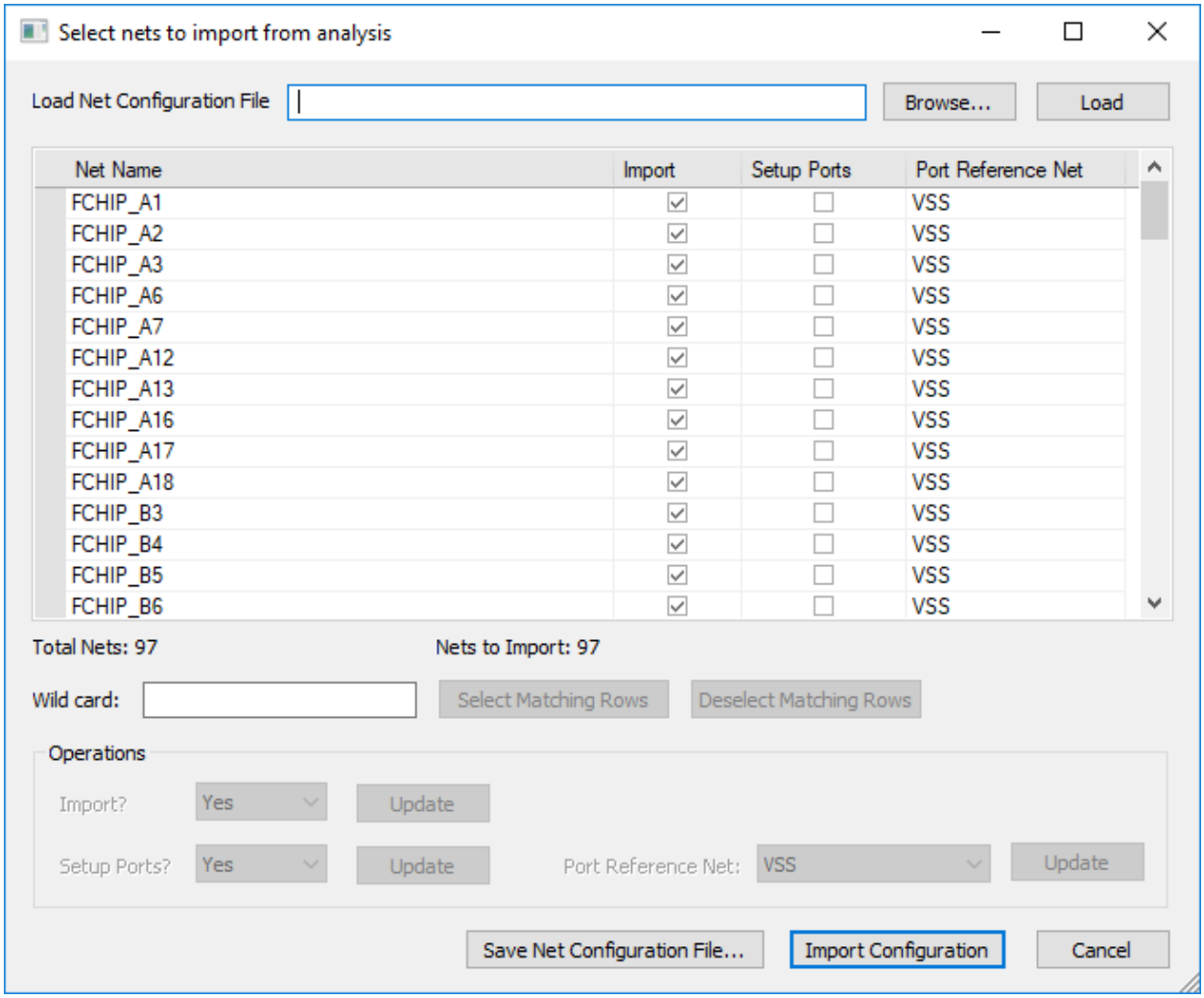
To begin, import the package design from an Ansys Neutral File (ANF).

These project files contain information about the geometry, layer stackup, padstacks, via construction, and discrete components.

1. Launch **SIwave**.
2. If the **Welcome to SIwave** window opens at launch, close it.
3. Click the **Import** tab.
4. In the **Ansys EDA Layouts** area, click **ANF**.

   The **Select Ansoft Neutral File to Import** window appears.
5. Depending on your Operating System, browse to one of the following locations:
   - Windows: **\Program Files\ANSYS Inc\v251\AnsysEM\Win64\Examples\SIwave**
   - Linux: **/Program Files/ANSYS Inc/v251/AnsysEM/Linx64/Examples/SIwave**
6. Select the file **analysis.anf**.
7. Click **Open**.

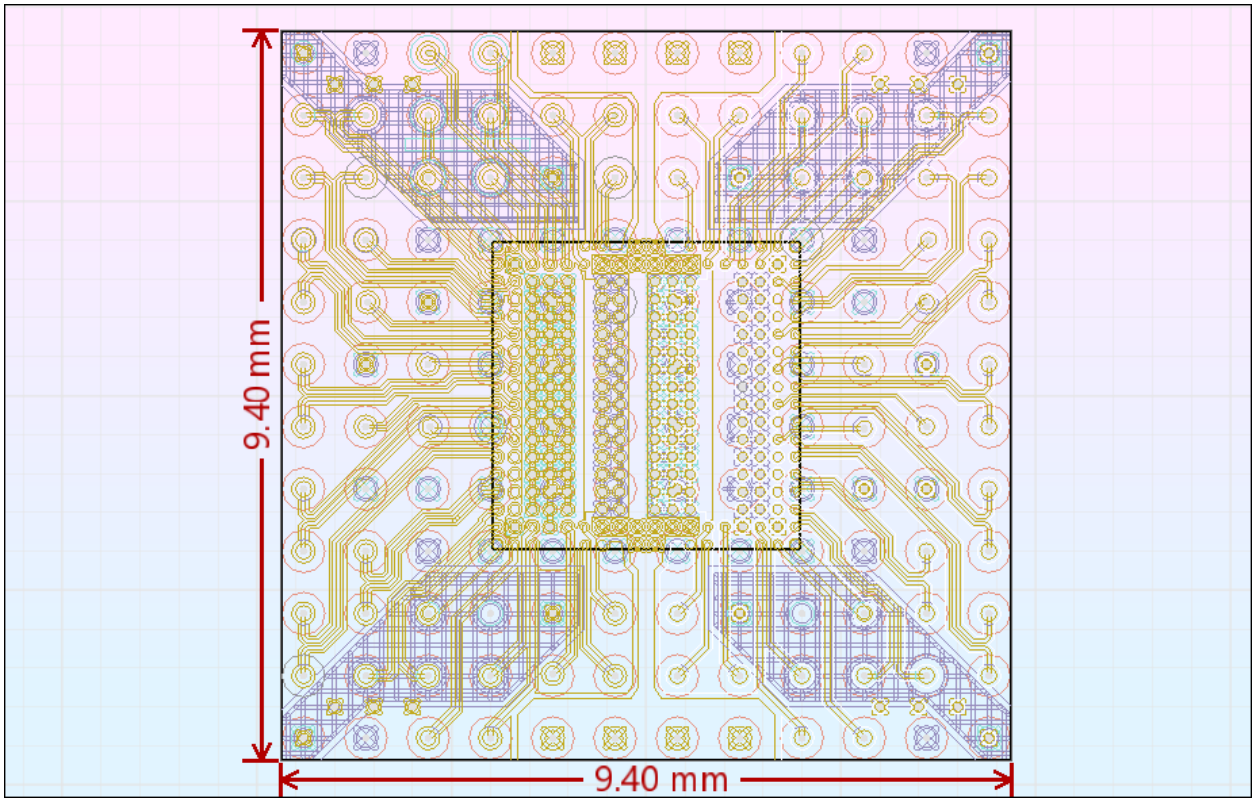
   The **Select nets to import from analysis** window appears.



8. Leave the settings as they are, and click **Import Configuration** to import the component file for the project's components.

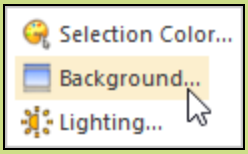
   If a **Component Import Overwrite** message appears, click **Yes to All** to overwrite any existing names.

   The project loads, and the SIwave desktop should look like the following:



Note:

You can change SIwave's background colors from the **View** tab:



If the **SIwave Workflow Wizard** window appears in front of your workspace, close it.

9. Click **File** > **Save As**.

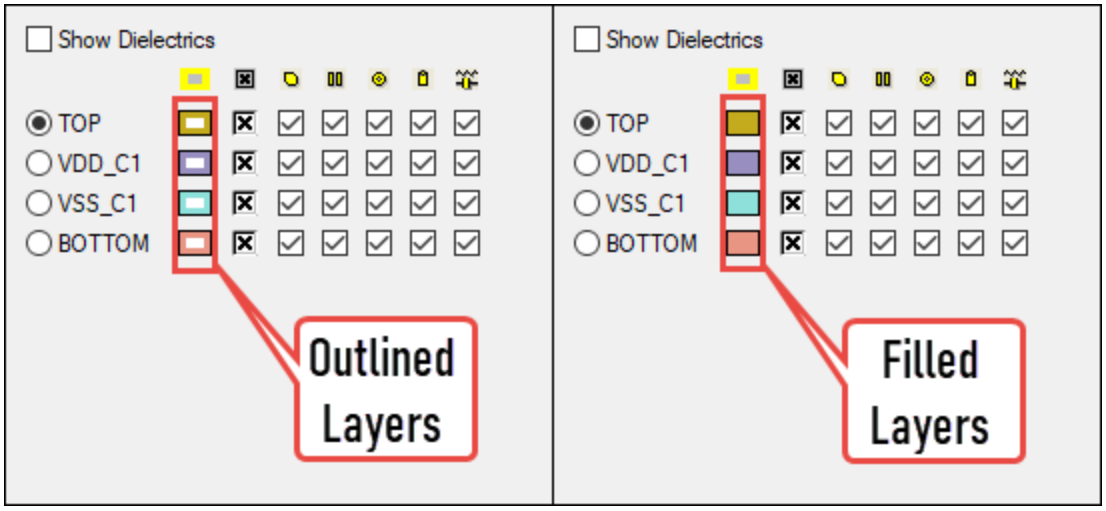
   The **Save As** window appears.

10. Browse to a directory where you have write permission. Give the project a name (e.g., **analysis.siw**).
11. Click **Save**.

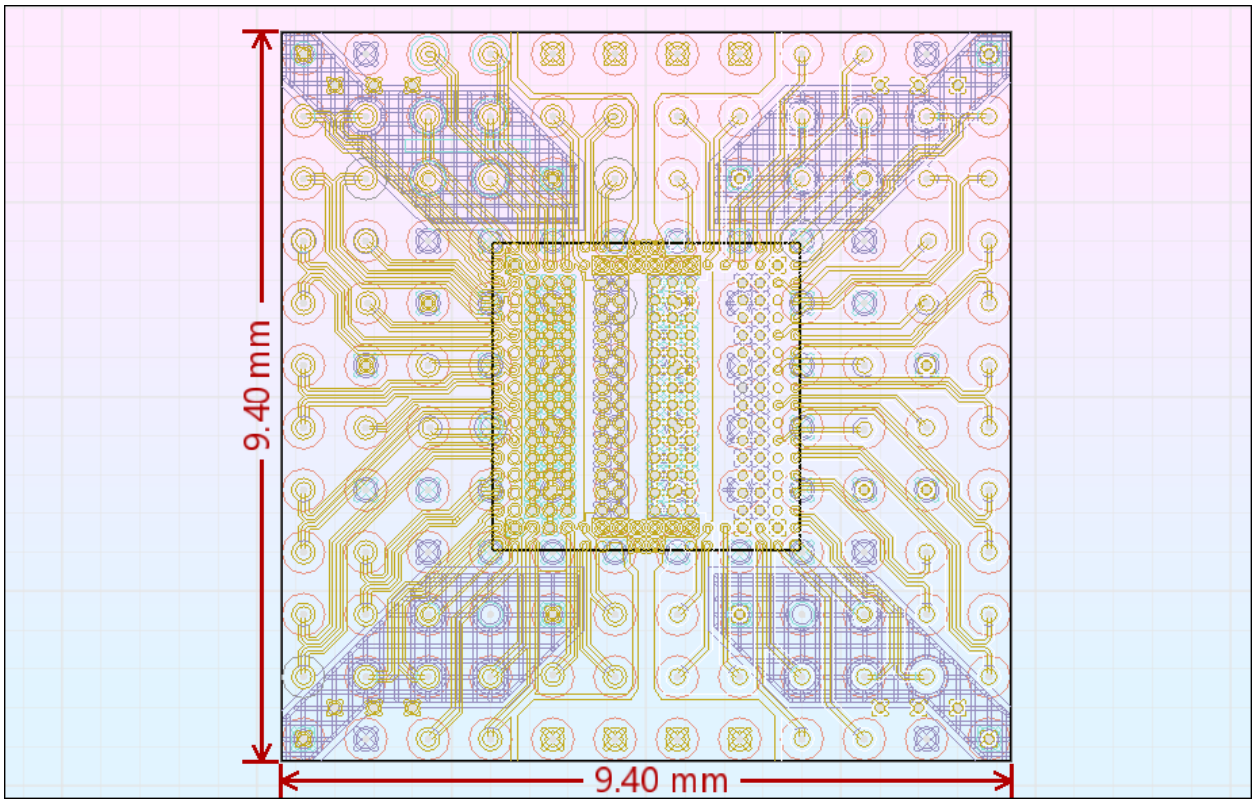
Working with Layers

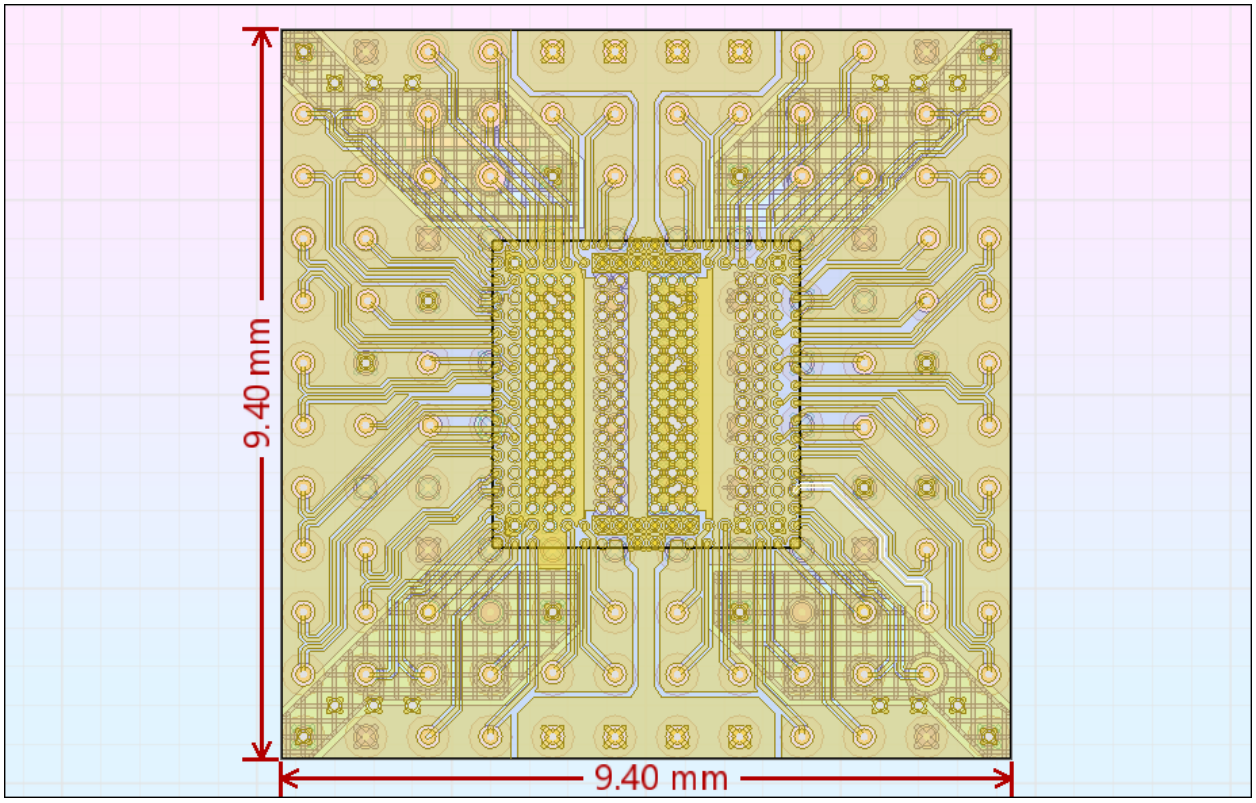
The Layers workspace and the Layer Stackup Editor control the visibility and properties of the package layers.

1. In the **Layers** workspace at the upper right of the SIwave window, use the check boxes in the **Show All/Hide All** column ( ) to turn on full visibility for all layers.
2. Click within the colored rectangles to change each layer from outline to solid fill.



The images below show how filling layers changes the display in the modeling workspace.

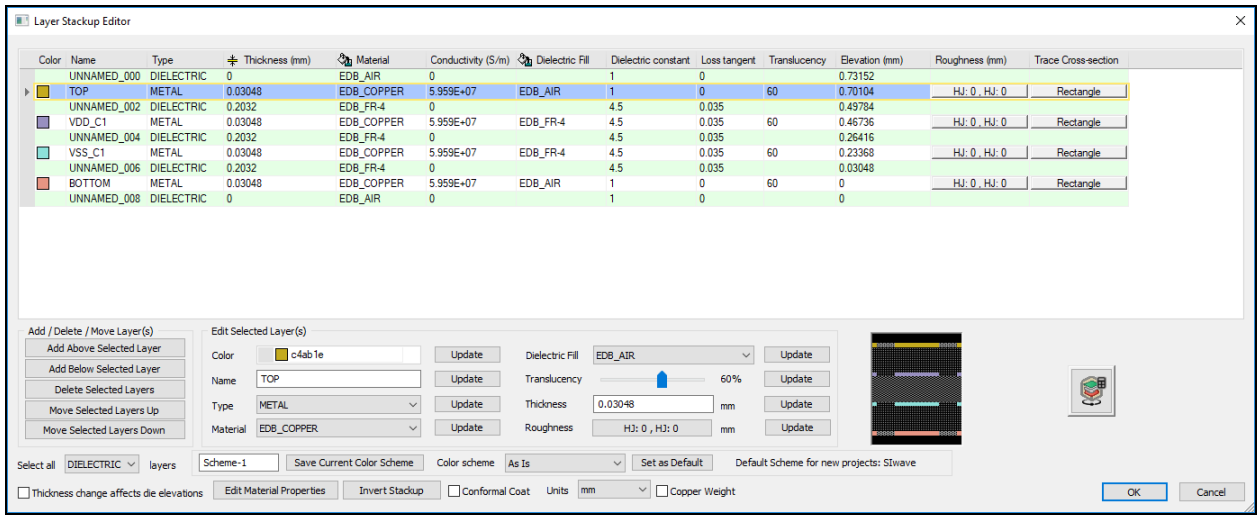




There are no layer changes necessary for this SIwave-CPA analysis, but if there were, you would make them using the **Layer Stackup Editor**.

3. Click **Home** > **Layer Stackup Editor** to review these settings.

   The **Layer Stackup Editor** appears.



4. Click **OK** to exit the **Layer Stackup Editor**.

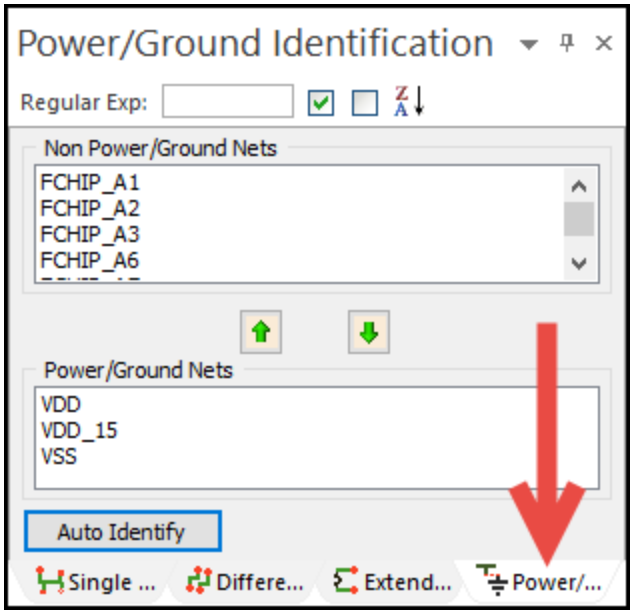
Identifying Power and Ground Nets

Nets containing large planes must be classified as Power/Ground nets. Signal nets containing microstrip and stripline routing need to be classified as Non Power/Ground nets. This enables the solver to judiciously choose the mesh refinement and optimization strategies for the signal and power/ground nets.

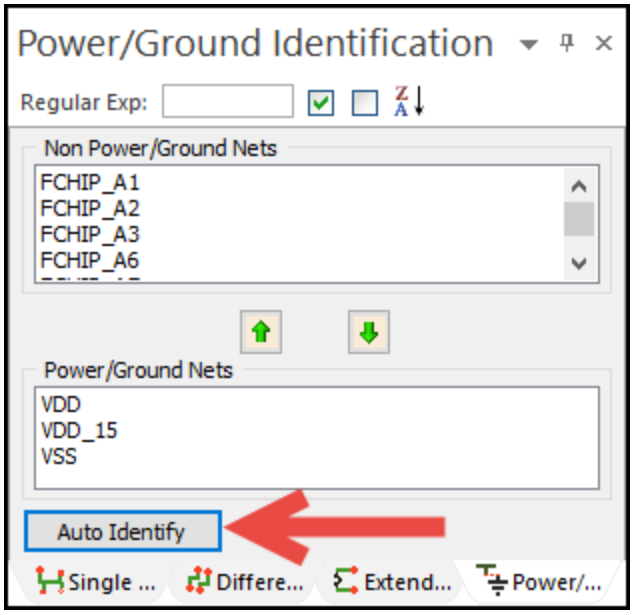
In this section, you will explore the **Nets** workspace.

> **Note:**
>
> By default, the **Nets** workspace is located on the upper-left side of the SIwave window. Workspaces can be moved by dragging and dropping them to another location.

1. In the **Nets** workspace, which defaults to **Single Ended Nets**, select the **Power/Ground Identification** tab.



2. Click **Auto Identify** to have SIwave automatically classify the power and ground nets.



Nets **VDD**, **VDD_15**, and **VSS** should be classified as **Power/Ground Nets**.

3. If any net is incorrectly identified, click to highlight the net name and use the up and down arrows to move it to the correct list.

3 - SIwave-CPA RLGC Extraction

This section explains how to perform the following tasks:

- Defining pin groups on power and ground nets
- Performing an RLCG extraction

Defining Pin Groups on Power/Ground Nets

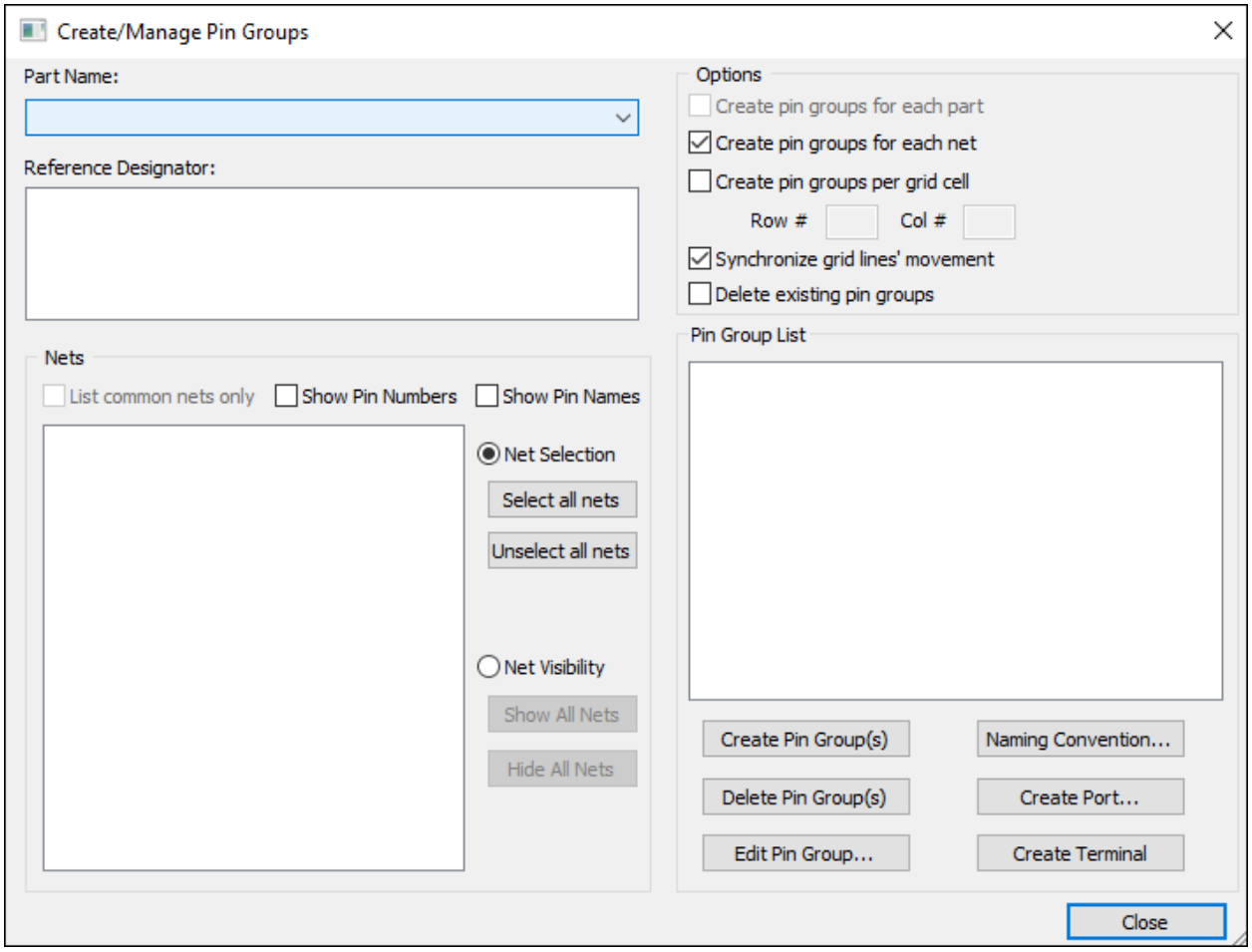
CPA extraction is controlled by the pin groups defined in the project.

When a RedHawk PLOC file is imported into SIwave, it creates pin groups and these are subsequently used for extraction.

Otherwise, pin groups must be created manually, as in the next steps.

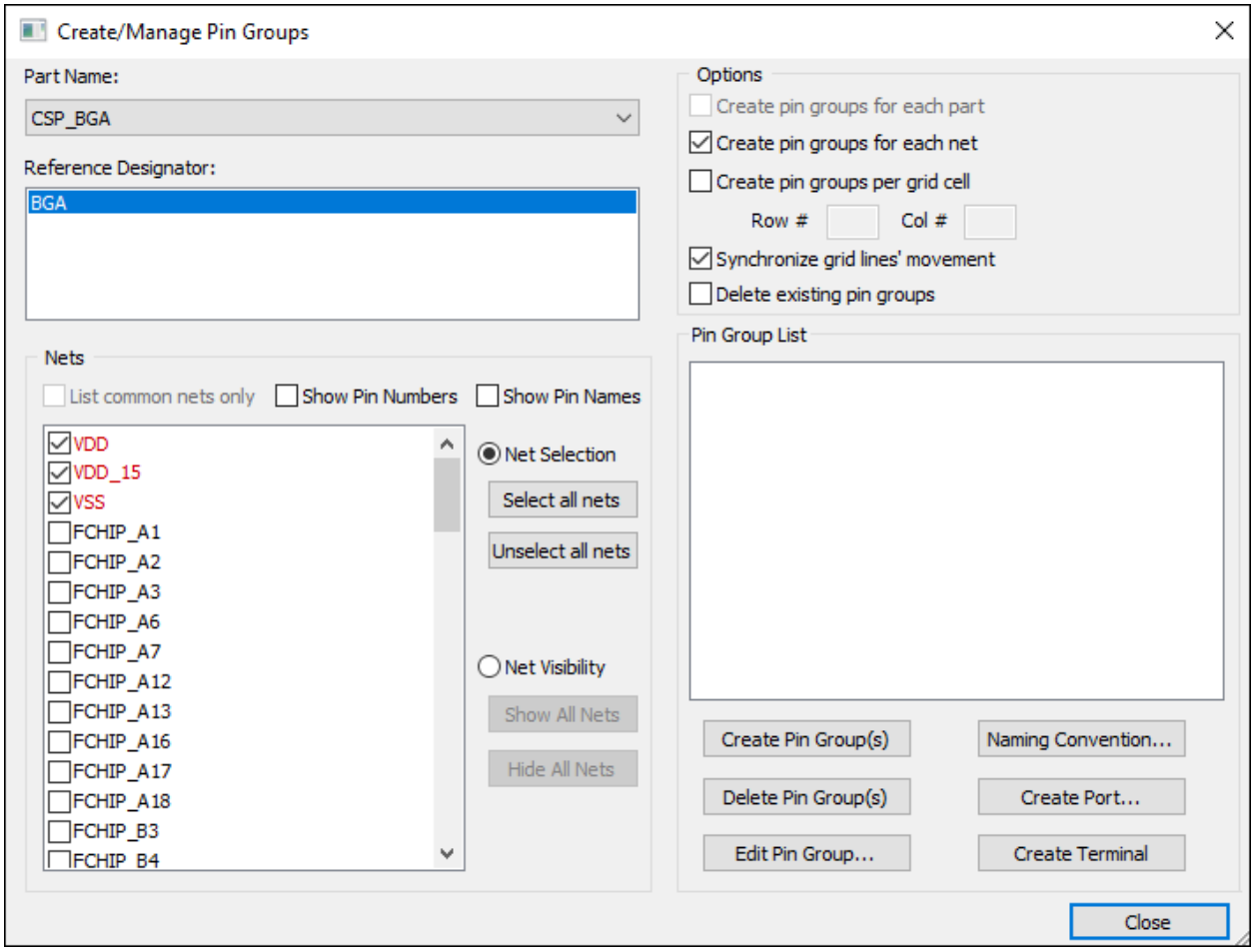
1. Click **Tools** > **Create/Manage Pin Groups**.

   The **Create/Manage Pin Groups** window appears.



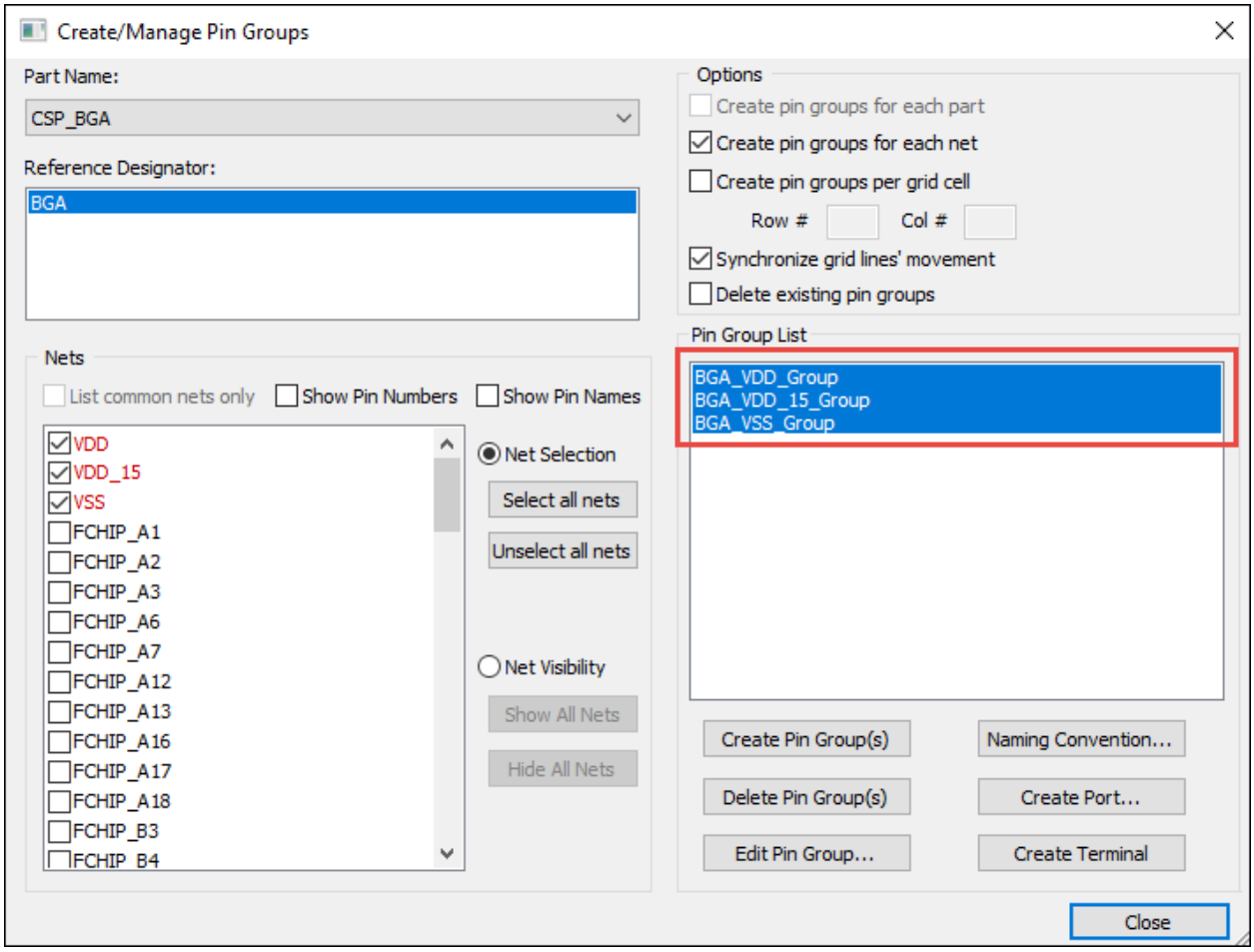
2. From the **Part Name** drop-down menu, select part name **CSP_BGA**.
3. From the **Reference Designator** list, select **BGA**.
4. From the **Nets** list, ensure that **VDD**, **VDD_15**, and **VSS** are selected. Ensure that the **Create pin groups for each net** check box is selected.

   The settings should look like the following:

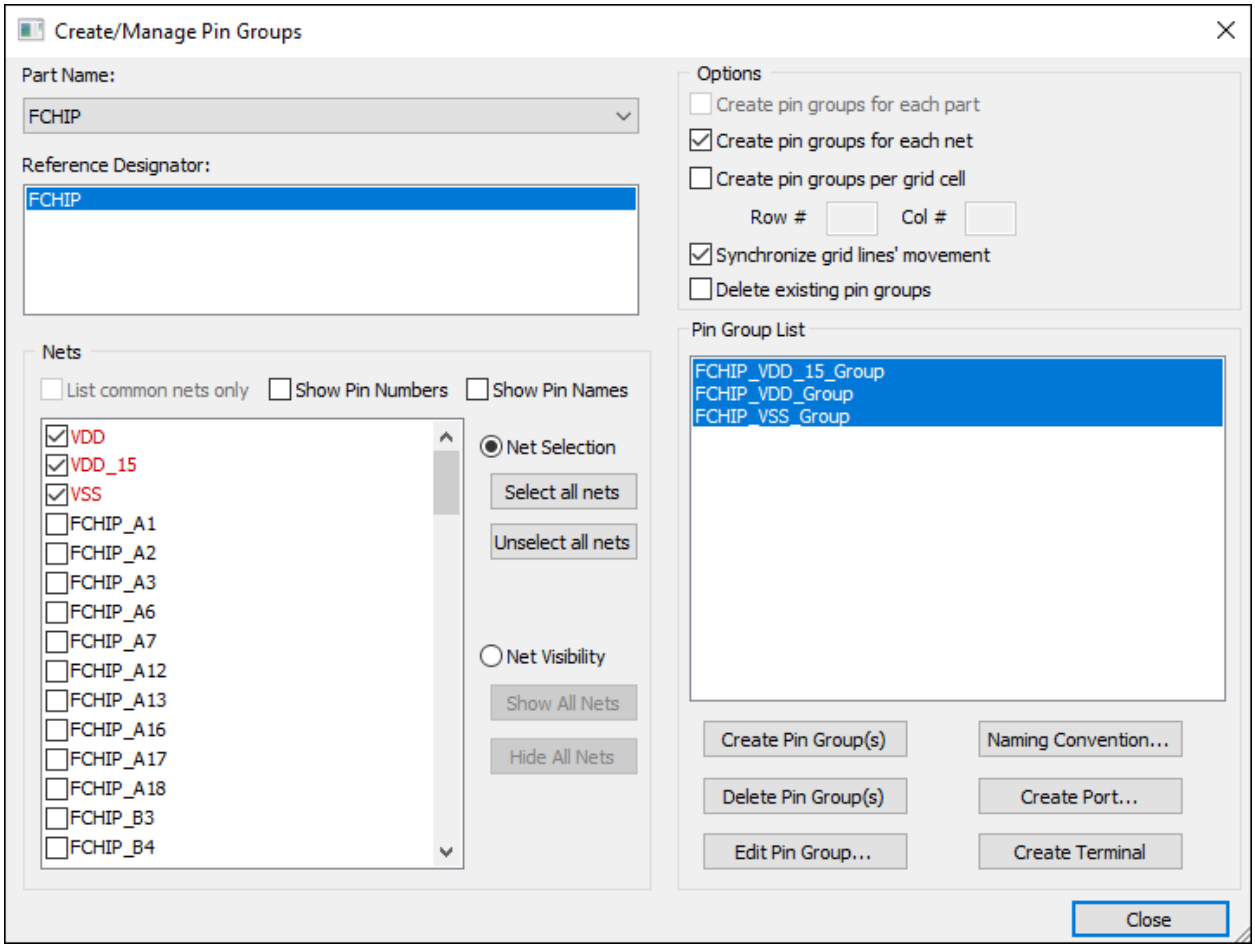


5. Click **Create Pin Group(s)**.

   You can now see the three pin groups listed.



6. In the **Part Name** drop-down menu, select **FCHIP**. In the **Reference Designator** field, select **FCHIP**.
7. Repeat steps 4 and 5 to create pin groups on the die for **VDD**, **VDD_15**, and **VSS**.



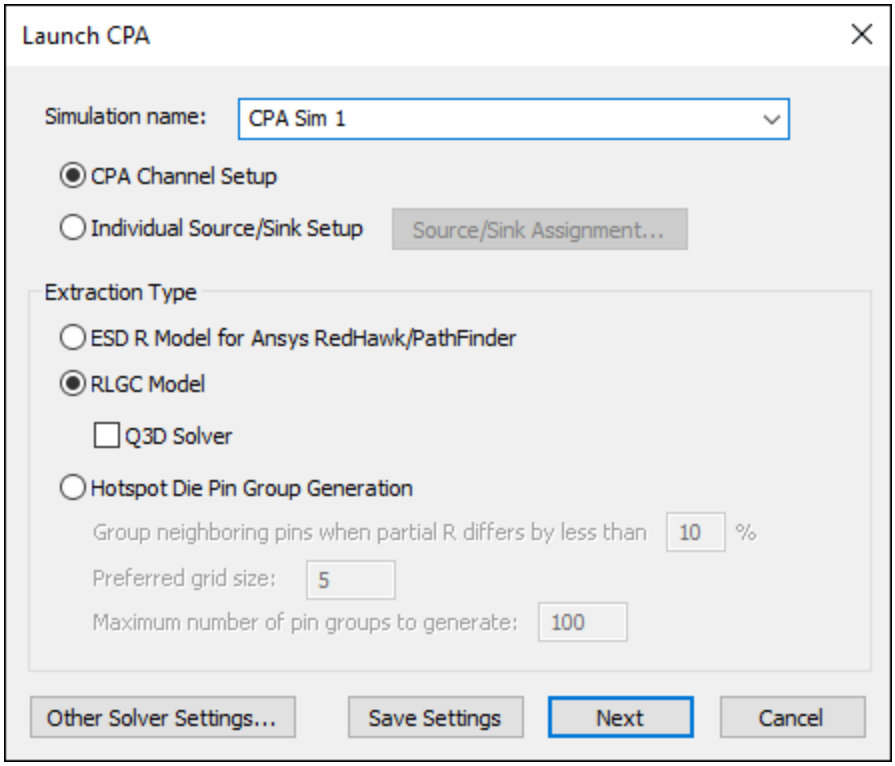
8. Click **Close**.

With pin groups created, the design is ready for RLGC Extraction.

Performing RLGC Extraction

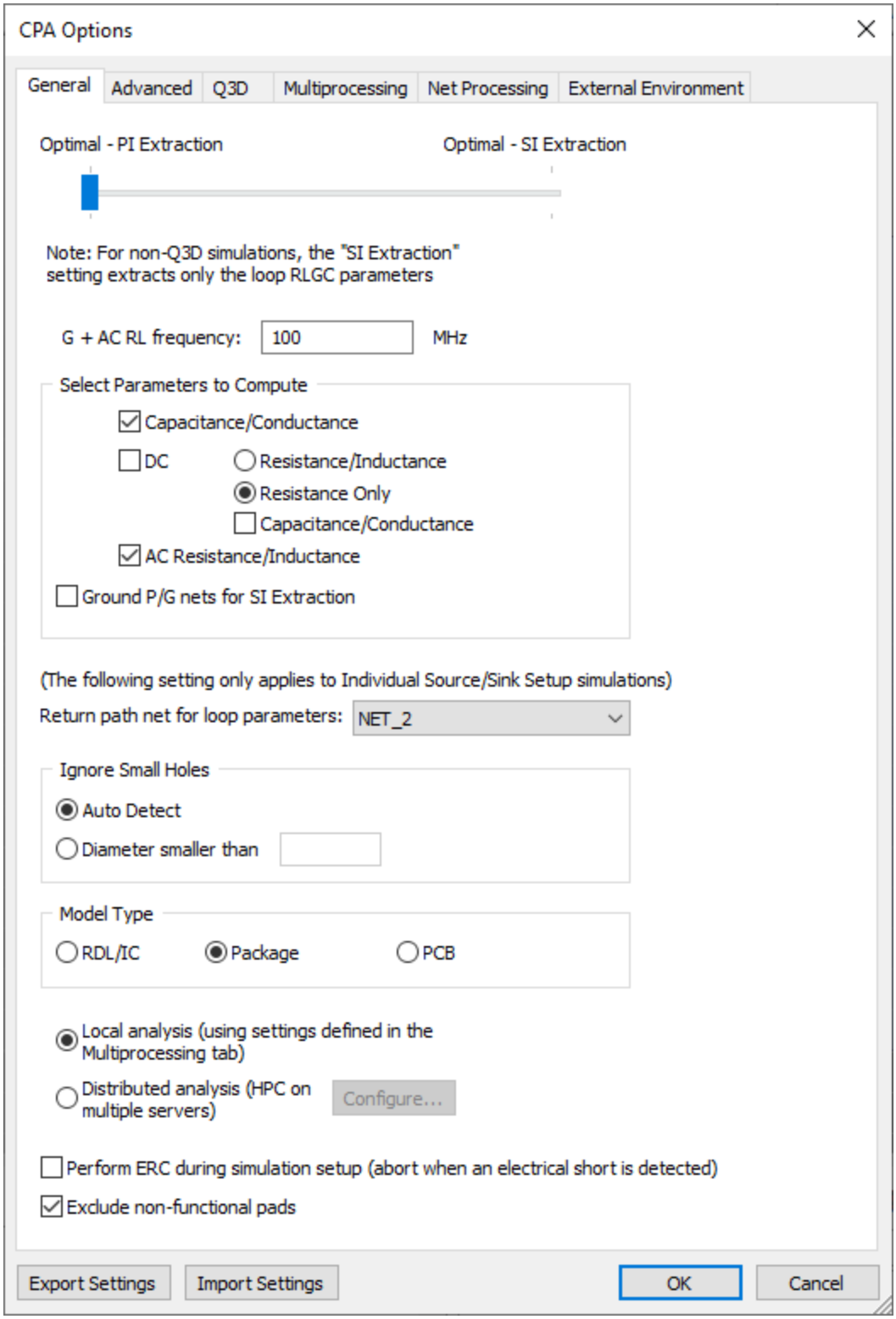
Follow the steps below to perform the simulation.

1. Navigate to the **Simulation** tab.
2. From the **CPA** area, click **Compute RLCG** to open the **Launch CPA** window.



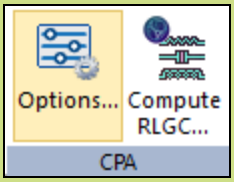
3. Accept the default settings, which should include the following:
   - **CPA Channel Setup** is selected.
   - **RLCG Model** is selected from the **Extraction Type** area.

4. Click **Other Solver Settings** to open the **CPA Options** window.



Note:

This window is also accessible directly from the **Simulation** tab. From the **CPA** area, click **Options**.

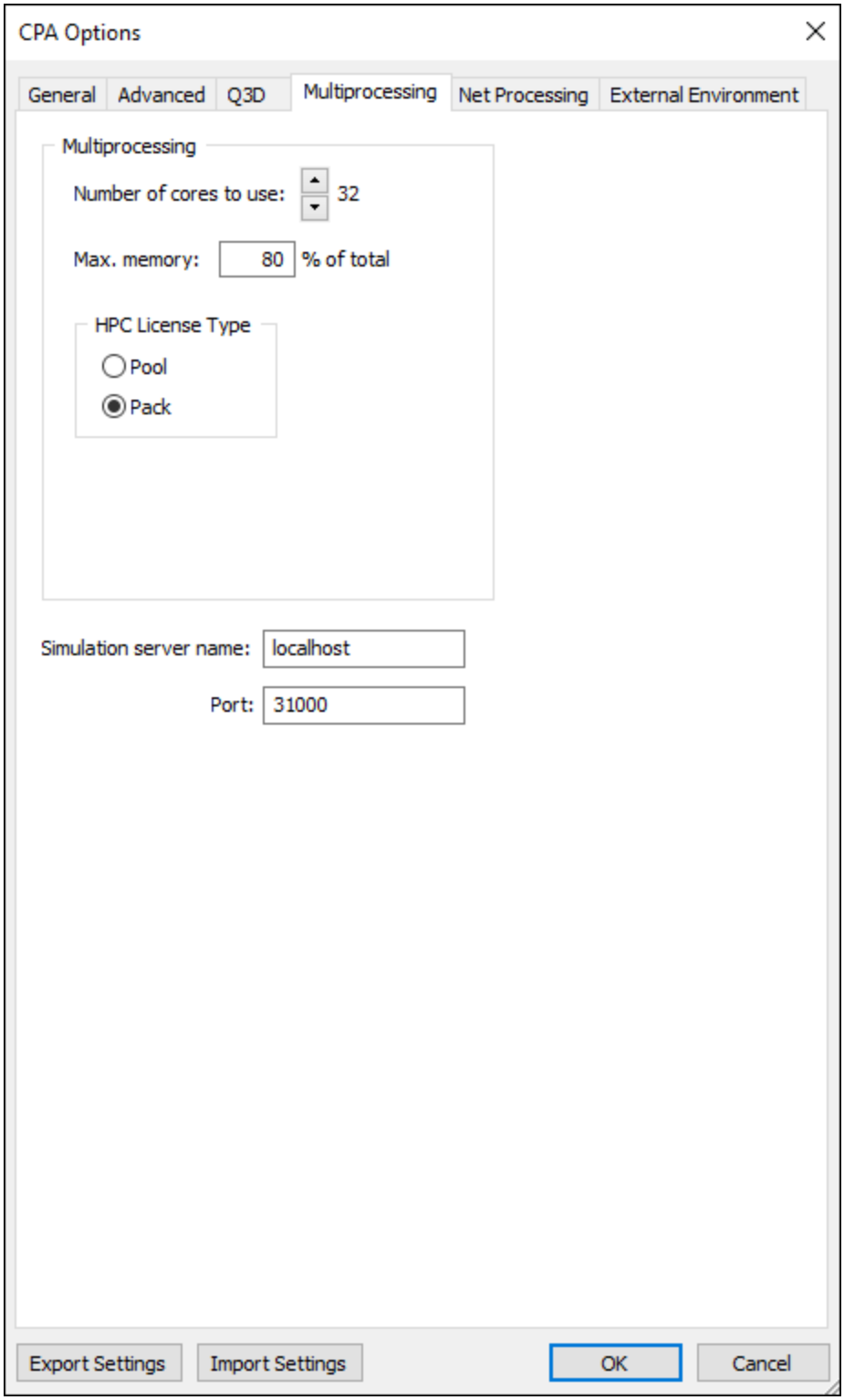


5. Ensure that the **Model Type** is set to **Package**.

Note:

- The CPA Channel Setup model, without Q3D Solver selected, automatically solves for all parameters (e.g., DC R, AC RL, CG, etcetera.) even if the boxes are not selected. These parameters are needed as the model must be RedHawk compatible.
- **Select Parameters to Compute** options only apply when **Individual Source/Sink Setup** or **Q3D Solver** was selected on the previous window.
- Adaptive Refinement settings are only respected when the **Q3D Solver** option was selected on the previous window.

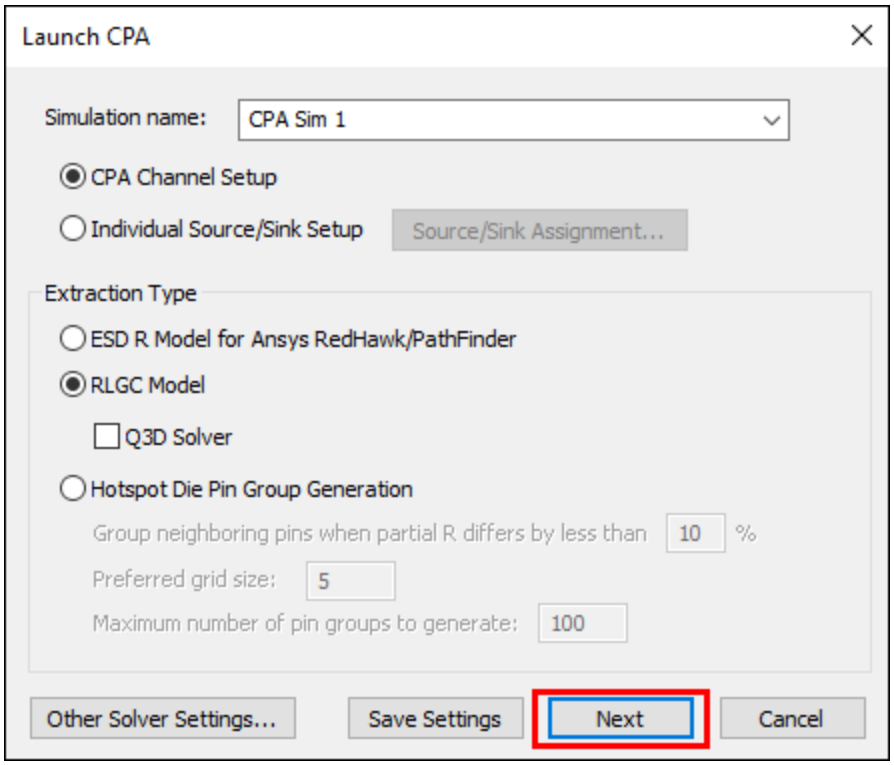
6. Click the **Multiprocessing** tab.



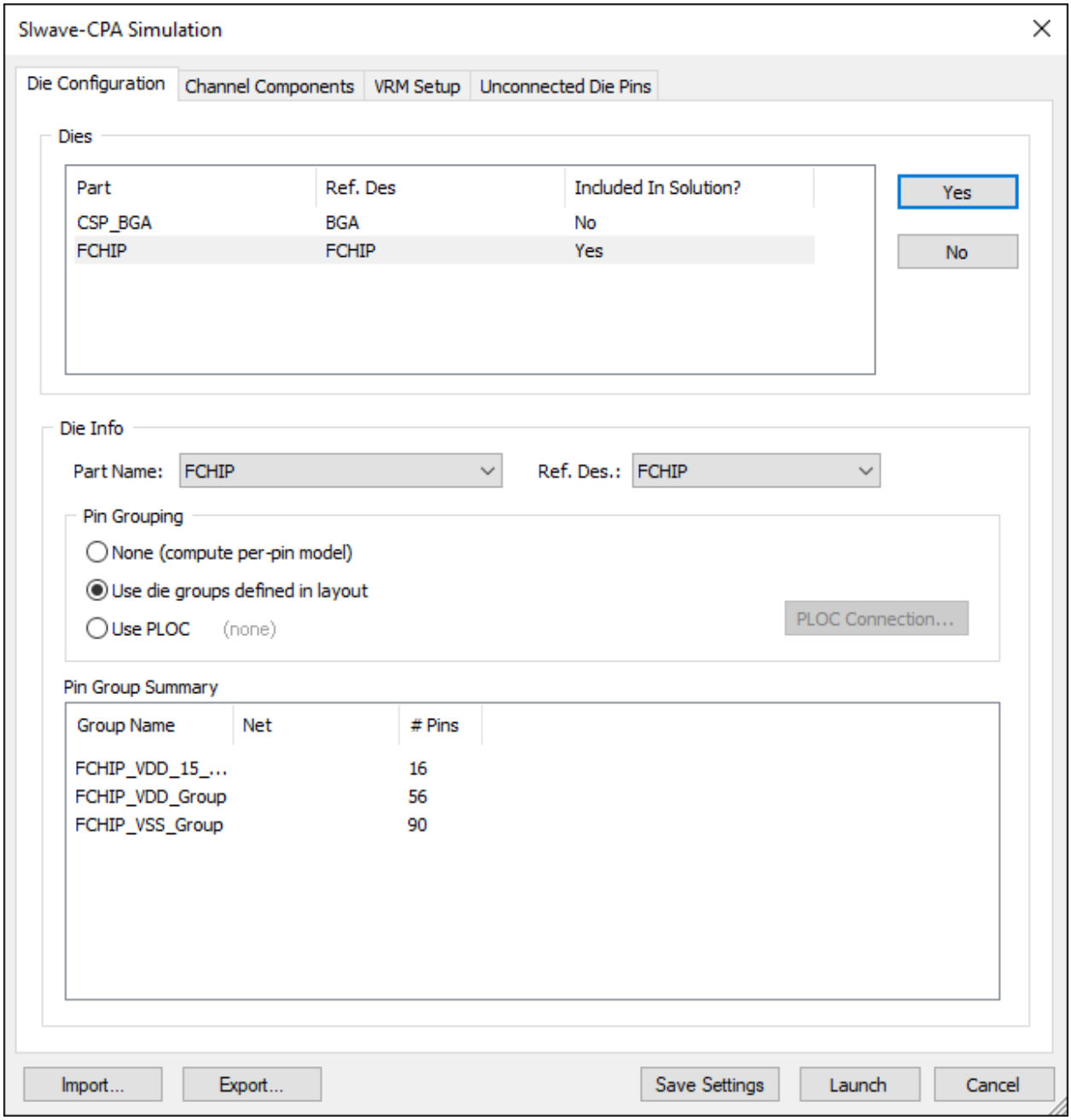
7. Use the up (∧) and down (∨) buttons to change the number of cores to use. To use all cores, press the up button until you cannot go any higher.

> **Important:**
>
> At least 8, and optimally 12-16 cores are recommended for best performance.

8. Click **OK** to close the **CPA Options** window and return to the **Launch CPA** window.
9. In the **Launch CPA** window, click **Next**.



The **SIwave-CPA Simulation** window appears, on the **Die Configuration** tab.



10. From the list of **Dies**, select **FCHIP**. Using the **Yes** button, ensure that **Included in Solution?** is set to **Yes**.
11. Under **Pin Grouping**, ensure that **Use die groups defined in layout** is selected.
12. Click **Launch**.

    The simulation begins and is tracked by a progress bar in the **Messages** workspace.

4 - Viewing CPA RLGC Results

This section explains how to perform the following tasks:

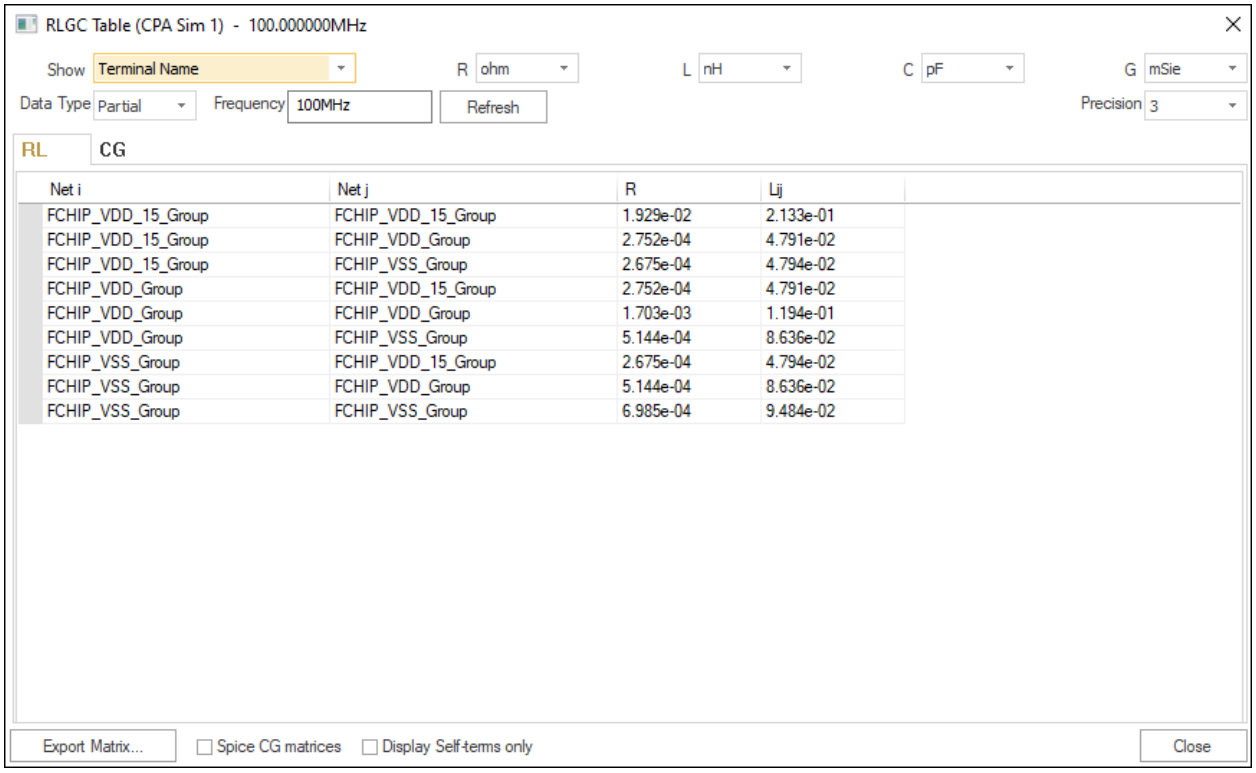
- Viewing tabular and SPICE results
- Viewing graphical results

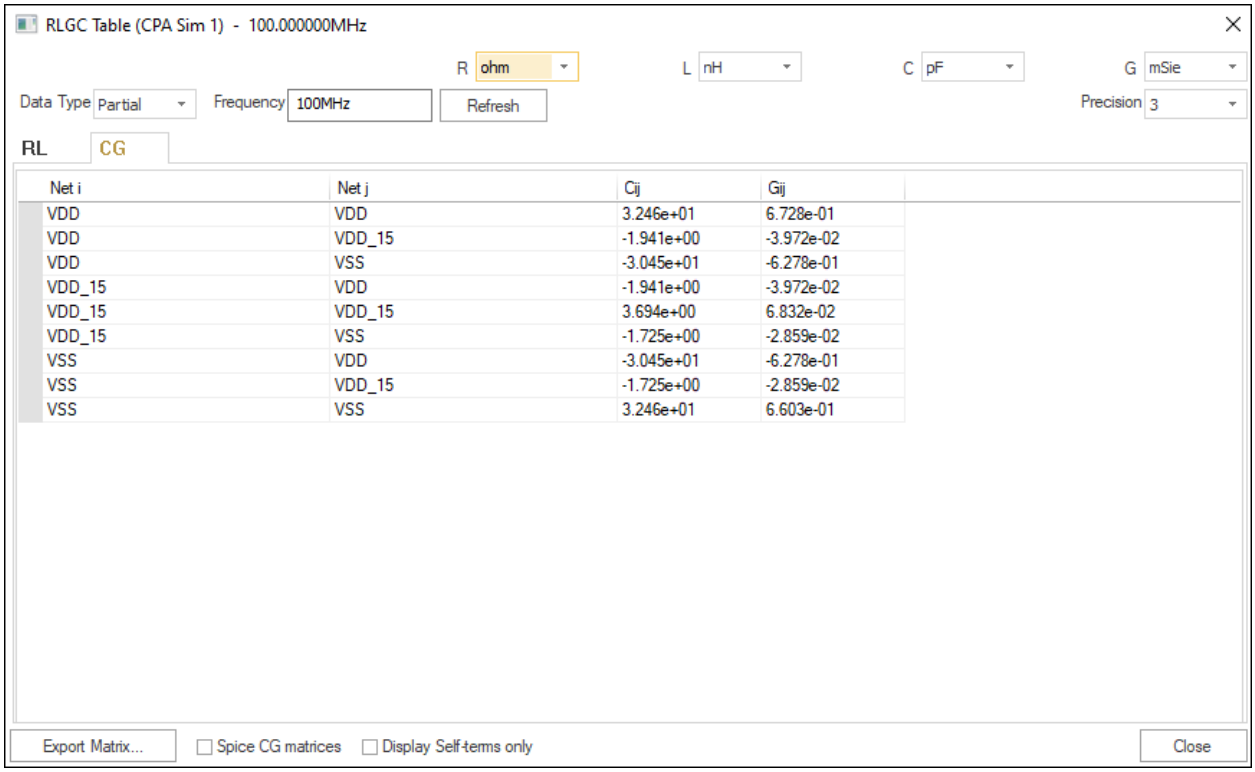
Viewing Tabular and SPICE Results

To view tabular results:

1. Click **Results**.
2. In the **CPA** section, select **RLGC** > **CPA Sim1** > **RLGC Table**.

   The **RLGC Table** window appears, with tabs for **RL** and **CG**.





3. Click **Close**.

To view SPICE results:

1. View the result files in your Documents folder (or wherever you have set SIwave to save results) in the subfolder path:

   analysis.siwaveresults/0000_CPA_Sim_1/adsCPA/Extraction

File	Description
cpa_rh_pkg_wrapper_ASCII.sp	Top-level SPICE netlist
cpa_rh_pkg_wrapper.sp	Encrypted wrapper for RedHawk
mult_whole.lvl	AC RLCG data
mult_whole_dcres.lvl	DC RLCG data
RLCG_Consolidate.txt	Consolidated RLCG data
cpa_annotated*.ploc	ASCII and encrypted PLOC files for system level connectivity
0000_CPA_Sim_1.sp	Package RLCG netlist

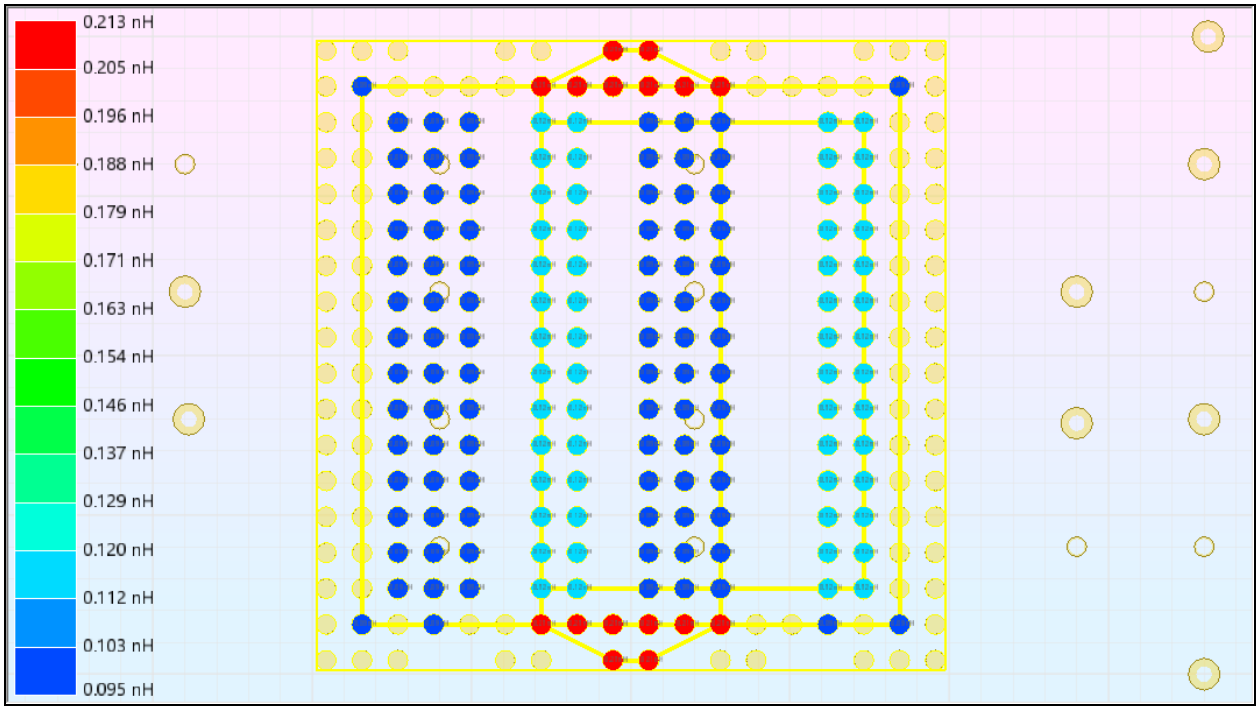
File	Description
Loop_L.txt	Loop inductance for all extracted components
0000_CPA_Sim_1.pkg	Package IBIS model
Cmatrix.txt, Gmatrix.txt	Maxwell CG matrices

Viewing Graphical Results

To view graphical results:

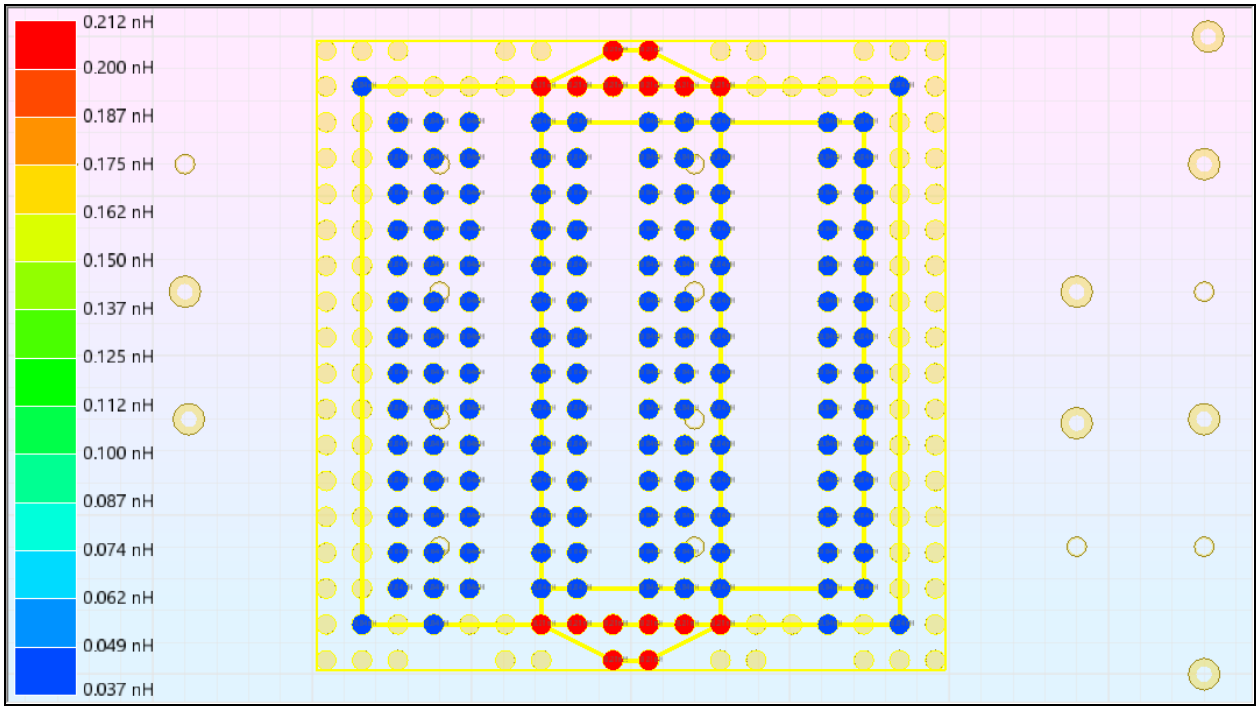
1. Click **Results**.
2. In the **CPA** section, click **Results** > **RLGC** > **CPA Sim1** > **Plot pin RL** > **Plot pin partial inductance map**.

   A color map display of each pin group's partial inductance is shown, superimposed over the FCHIP component.



3. In the **CPA** section, click **Results** > **RLGC** > **CPA Sim1** > **Plot pin RL** > **Plot pin loop inductance map**.

   A color map display of each pin group's loop inductance is shown, superimposed over the FCHIP component.



4. Save the project to retain the RLCG extraction result.
5. Close the project and exit SIwave.